

# NUP2114 Series, SNUP2114UCMR6T1G

## Transient Voltage Suppressors

### Low Capacitance ESD Protection for High Speed Data

The NUP2114 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 applications.

#### Features

- Low Capacitance 0.8 pF
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- AEC-Q101 Qualified and PPAP Capable – SNUP2114
- Low Clamping Voltage
- Stand Off Voltage: 5 V
- Low Leakage
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:  
IEC 61000-4-2 Level 4 ESD Protection
- UL Flammability Rating of 94 V-0
- These are Pb-Free Devices

#### Typical Applications

- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Monitors and Flat Panel Displays
- MP3
- Gigabit Ethernet
- Notebook Computers
- Digital Video Interface (DVI) and HDMI

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact IEC61000-4-2 Air	ESD	16000 400 8000 15000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



ON Semiconductor®

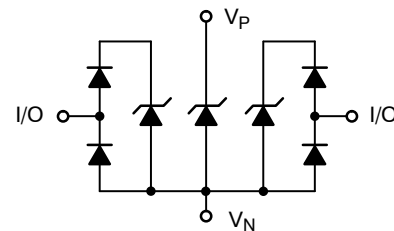
<http://onsemi.com>



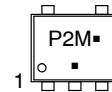
SOT-553  
CASE 463B



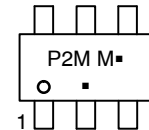
TSOP-6  
CASE 318G



#### MARKING DIAGRAMS



SOT-553

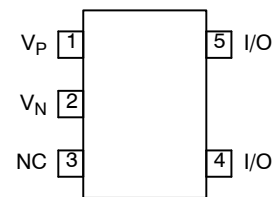


TSOP-6

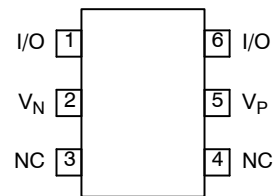
P2, P2M = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)

#### PIN CONNECTIONS



SOT-553



TSOP-6

#### ORDERING INFORMATION

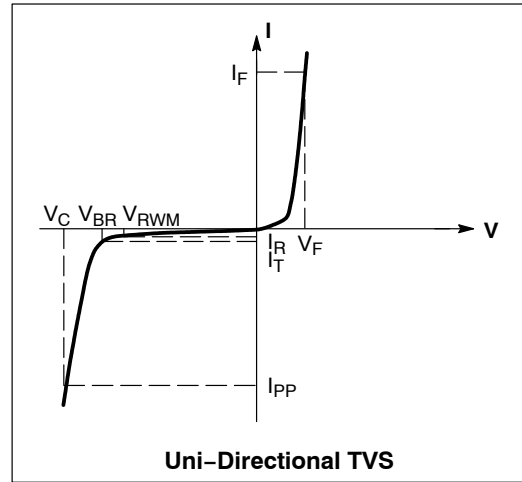
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# NUP2114 Series, SNUP2114UCMR6T1G

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz



\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

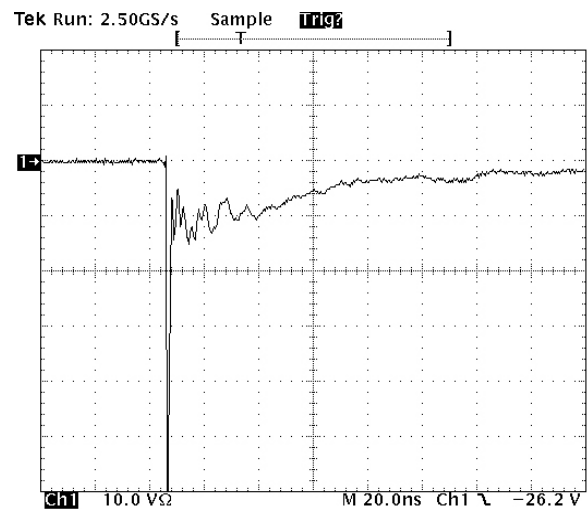
## ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 1)			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T = 1$ mA, (Note 2)	5.5	7.5		V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5$ V			1.0	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP} = 5$ A (Note 3)		9.0		V
Clamping Voltage	$V_C$	$I_{PP} = 8$ A (Note 3)		10		V
Maximum Peak Pulse Current	$I_{PP}$	8x20 $\mu\text{s}$ Waveform			12	A
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins and GND		0.8	1.0	pF
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins			0.5	pF
Clamping Voltage	$V_C$	@ $I_{PP} = 1$ A (Note 4)			12	V
Clamping Voltage	$V_C$	Per IEC 61000-4-2 (Note 5)	Figures 1 and 2			V

1. TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
2.  $V_{BR}$  is measured at pulse test current  $I_T$ .
3. Nonrepetitive current pulse (Pin 5 to Pin 2)
4. Surge current waveform per Figure 5.
5. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.
6. Include S-prefix devices where applicable.



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2**



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2**

# NUP2114 Series, SNUP2114UCMR6T1G

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

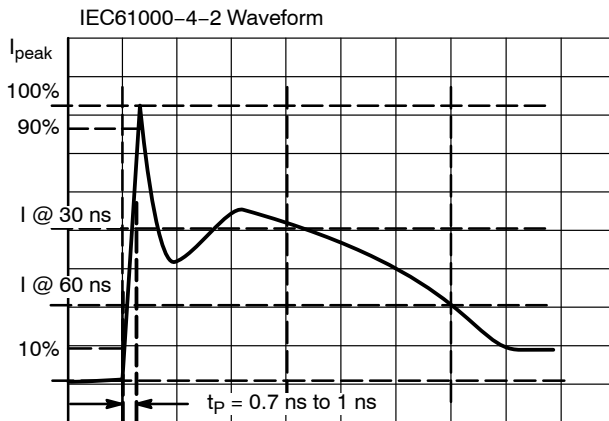


Figure 3. IEC61000-4-2 Spec

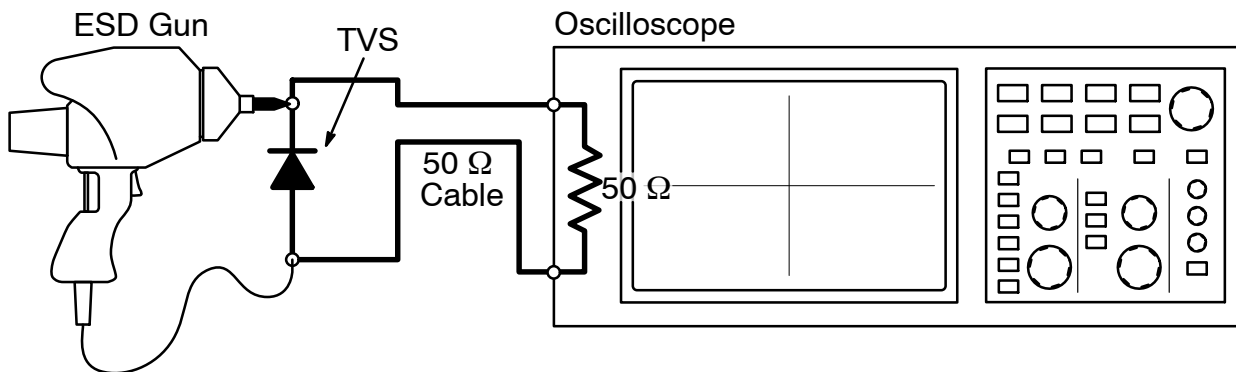


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

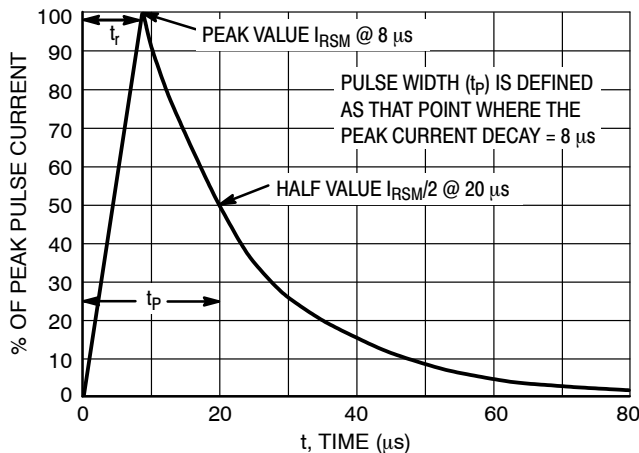


Figure 5. 8 X 20 μs Pulse Waveform

# NUP2114 Series, SNUP2114UCMR6T1G

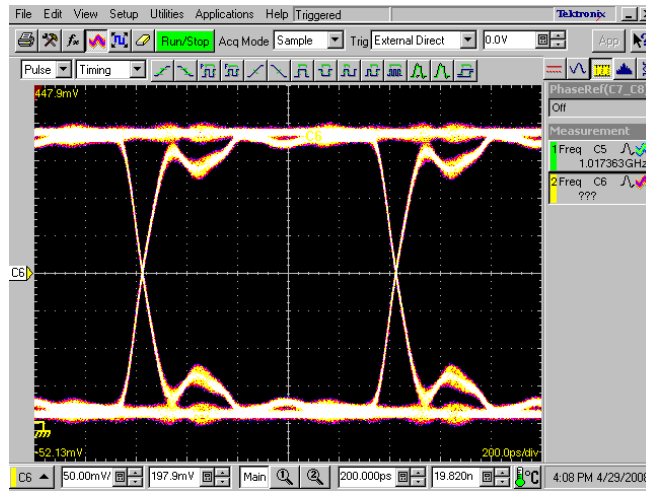


Figure 6. 500 MHz Data Pattern

## ORDERING INFORMATION

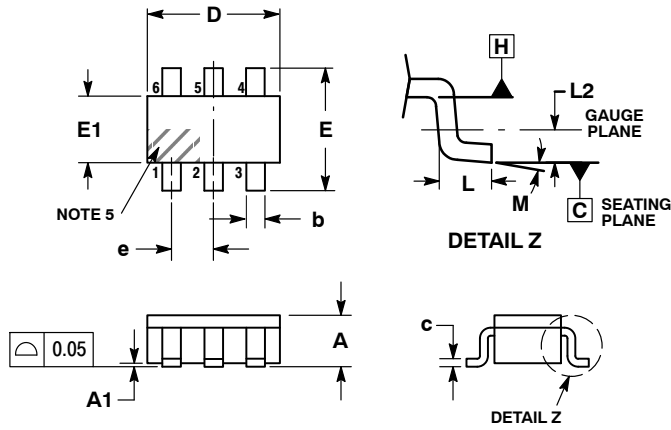
Device	Marking	Package	Shipping <sup>†</sup>
NUP2114UPXV5T1G	P2	SOT-553 (Pb-Free)	4,000 / Tape & Reel
NUP2114UCMR6T1G	P2M	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
SNUP2114UCMR6T1G	P2M	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NUP2114 Series, SNUP2114UCMR6T1G

## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE U

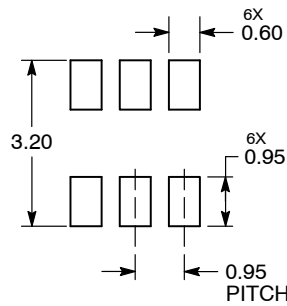


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

### RECOMMENDED SOLDERING FOOTPRINT\*



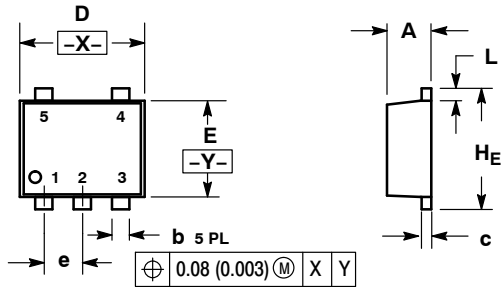
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NUP2114 Series, SNUP2114UCMR6T1G

## PACKAGE DIMENSIONS

### SOT-553, 6 LEAD CASE 463B-01 ISSUE B

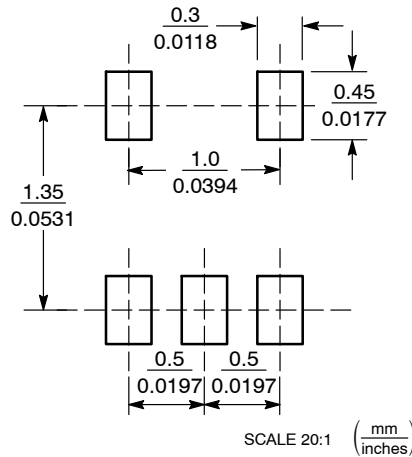


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NUP2114UCMR6T1G](#) [NUP2114UPXV5T1G](#) [SNUP2114UCMR6T1G](#)